Logic Analyser

for Embedded Interfaces analysis

The Discovery logic analyzer series, PGY-LA-EMBD has the built-in capability to debug I2C protocol, SPI protocol, UART, and many other serial protocols. This is a PC-based logic analyzer designed for professional engineers. The Discovery logic analyzer is used to debug embedded systems, the logic analyzer not only reduces the workbench area but also allows it to have a very small form factor and can be used to debug failures in the field. The protocol decode capabilities are designed to debug the logic and protocol issues faced by embedded design teams in the consumer, industrial, home automation, health, and education sectors.

PGY-LA-EMBD is an industry-first logic analyzer in its category which enables engineers to debug timing problems and perform simultaneous protocol analysis of I2C, SPI, UART or I3C, SPMI, and RFFE and also has support for CAN, CAN FD in embedded designs. This enables designers to debug circuit-level and system-level problems quickly.

PGY-LA-EMBD offers 1GS/Sec Asynchronous (timing) data and 100MHz Synchronous (state) data capture which makes it an ideal debug tool to address digital design problems. Designers can now easily analyze setup and hold time issues, glitches and synchronous data activities apart from analyzing protocol issues.

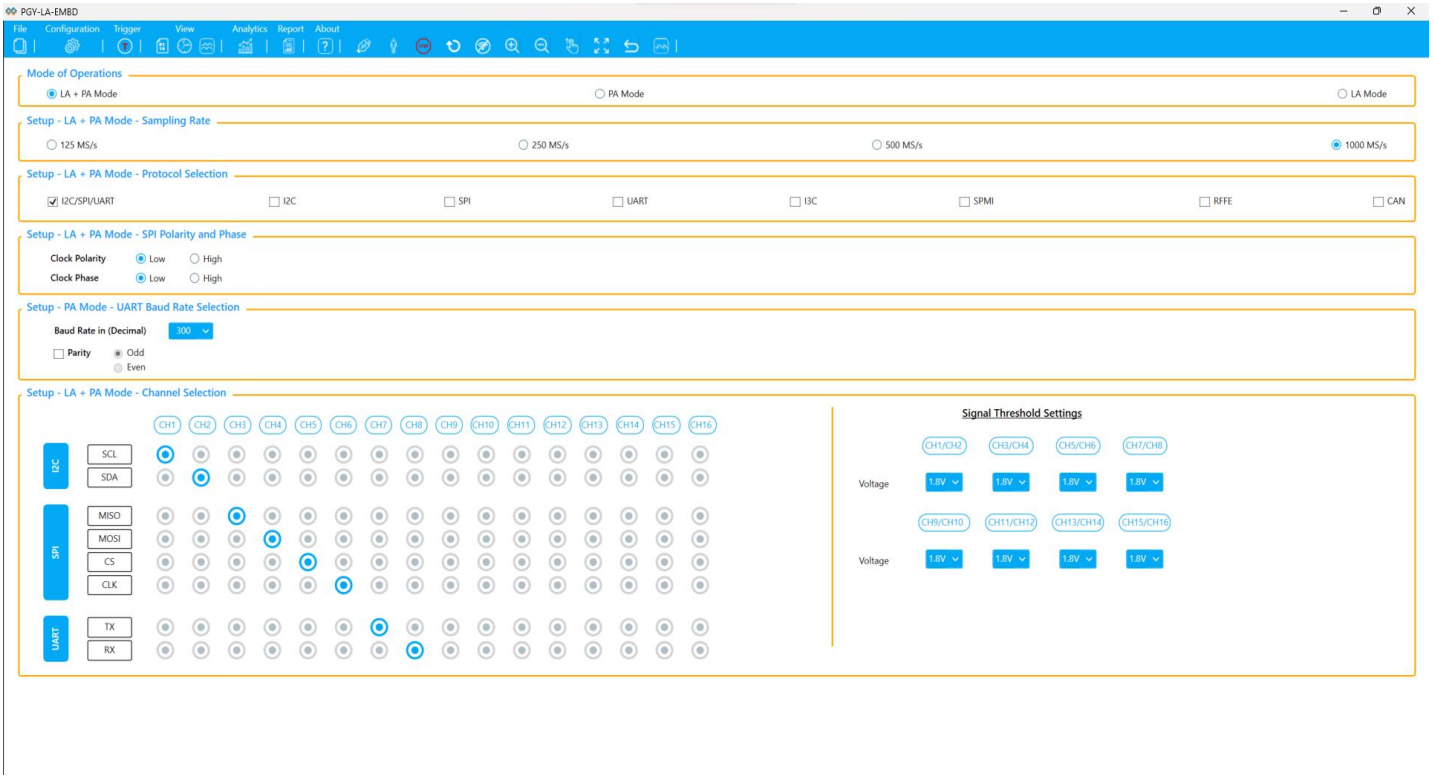
Current generation embedded designers need to collect data from multiple interfaces such as I2C, SPI, UART, I3C, SPMI, RFFE, CAN and , CAN FD and process it to achieve optimal performance of their design. Embedded design teams needs to take timely action to meet the intended objectives of the product. PGY-LA-EMBD decodes I2C, SPI, UART or I3C, SPMI, RFFE and CAN, CAN FD bus and displays the protocol activity with time stamp information. PGY-LA-EMBD is an ideal instrument to debug hardware and embedded software integration issues and optimize the software performance.

Multiple Markers enable smart delta measurements which are key to designers. Zoom enables users to look at specific areas of the signal.

Key Features
✧ 16 channels with Protocol and Logic Analysis capability. ✧ 1GS/Sec Timing (Asynchronous) Analysis. ✧ 100MHz State (Synchronous) Analysis. ✧ Simultaneous Protocol Analysis of I2C-SPI-UART and I3C-SPMI-RFFE and CAN, CAN-FD ✧ Detailed Trigger capabilities: Auto, Pattern, Protocol aware (I2C, SPI, UART, I3C, SPMI, RFFE, CAN) andTiming (Pulse Width and Delay Trigger). ✧ Smart streaming of data from Protocol Analyzer to host computer for long duration capture using USB 3.0 interface. ✧ Innovative easy to use Graphical user interface. ✧ Error Analysis of Protocol packet. ✧ Provides Timing, Waveform, Listing and Protocol listing views. ✧ Detailed filtering capability for protocol decoded data. ✧ PDF and CSV report format. ✧ API support.

Product SETUP

Easy To Configure

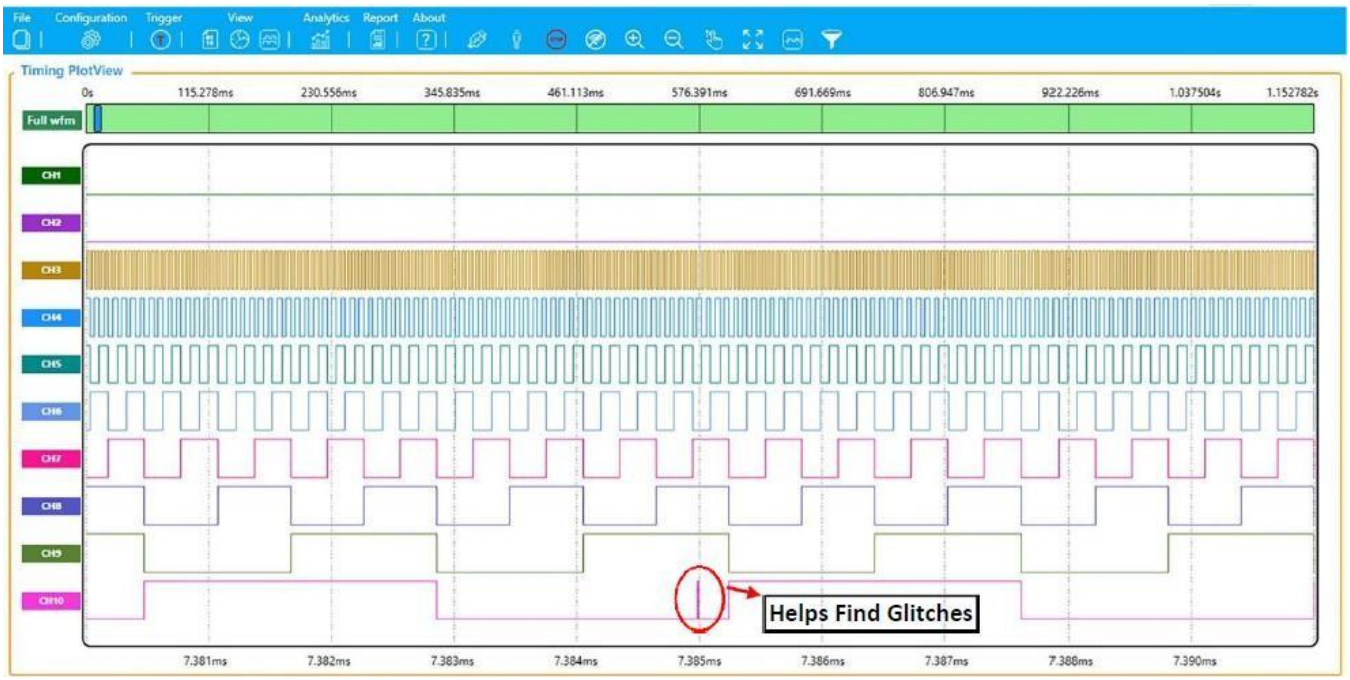


Users can easily configure the Logic Analyzer for embedded interfaces by either selecting Logic Analysis (LA) mode or Protocol Analysis (PA) mode or a combined (LA+PA) mode. This ensures a quick and easy way to configure the product and look at complex problems at system level either in Logic Analysis (State Analysis, Timing Analysis) or Protocol decoding or both. Save and Recall capability ensures designers can recall their custom setup details.

Multiple Domain

Multiple domain Views provide the necessary complete view of all supported interface states, timing and protocol activity. Users can easily setup the analyzer to view timing, logic and decode views to enable easy insights to the design. Users can set different trigger conditions from the setup menu to capture Timing and Protocol activity at specific events. The decoded results can be viewed in Timing, Logic and Protocol listing window with auto correlation. This comprehensive view of information makes it industry's best, offering an easy to use solution to debug the embedded interfaces protocol activity and analyze timing issues. Multiple cursors help designers to look into details of their design performance.

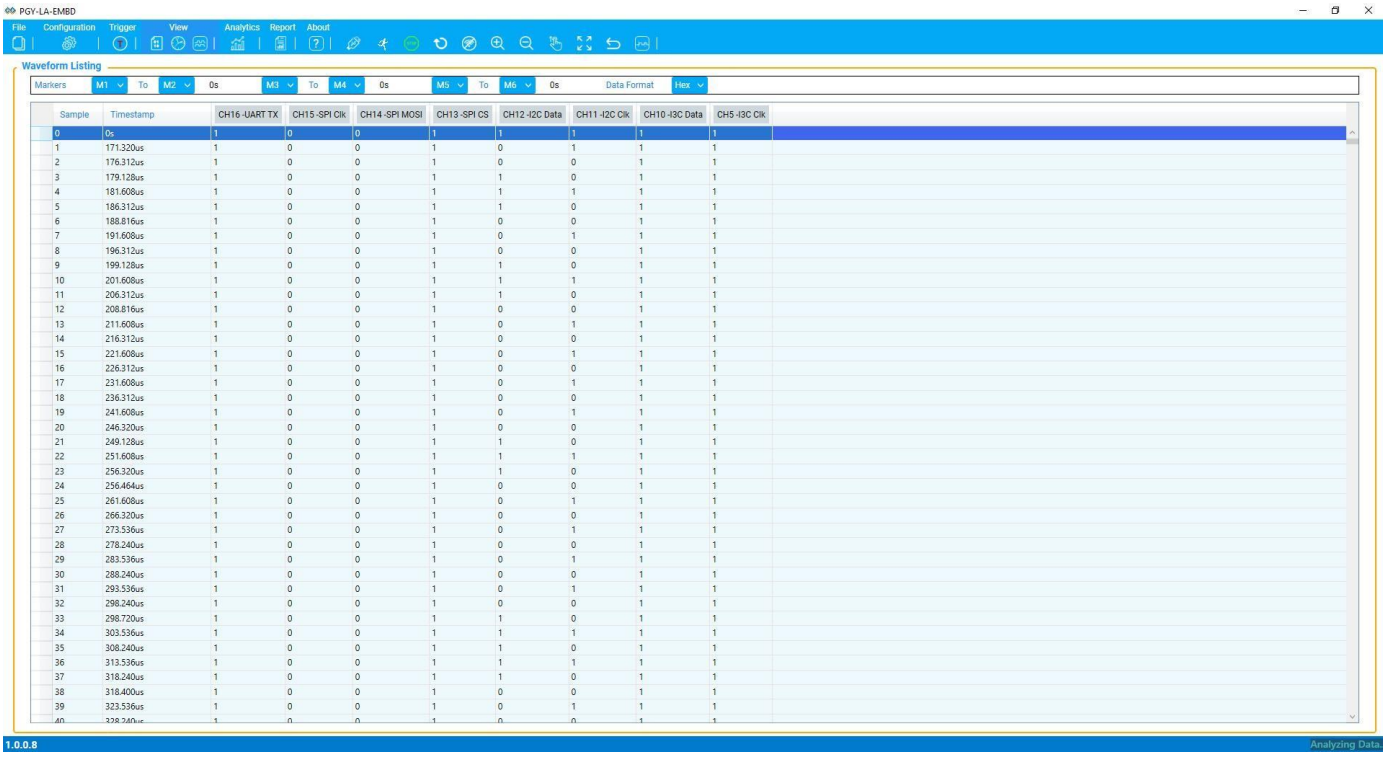
Timing View



Timing view is a unique capability of the PGY-LA-EMBD which enables designers to get detailed insights into their signal's timing information. The timing view uses an internal clock signal to plot the waveform. The flexible sampling rate selection enables designers to investigate Glitches that can cause issues in the functioning of their designs. The grouping feature enables designers to group various related signals for better viewing and analysis. Marker and Zoom features make it convenient to analyze any timing errors.

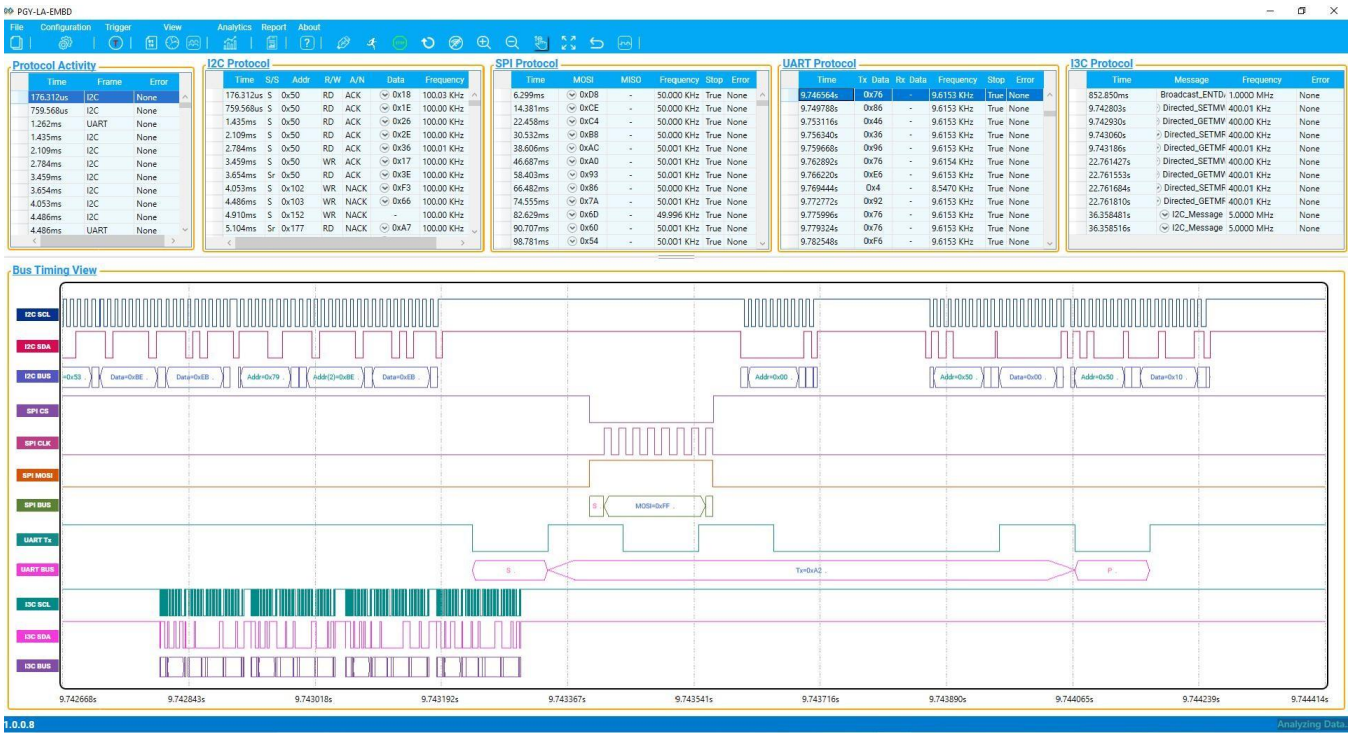
Ability to analyze any point in the captured data record ensures easy debugging and analysis over a long capture duration.

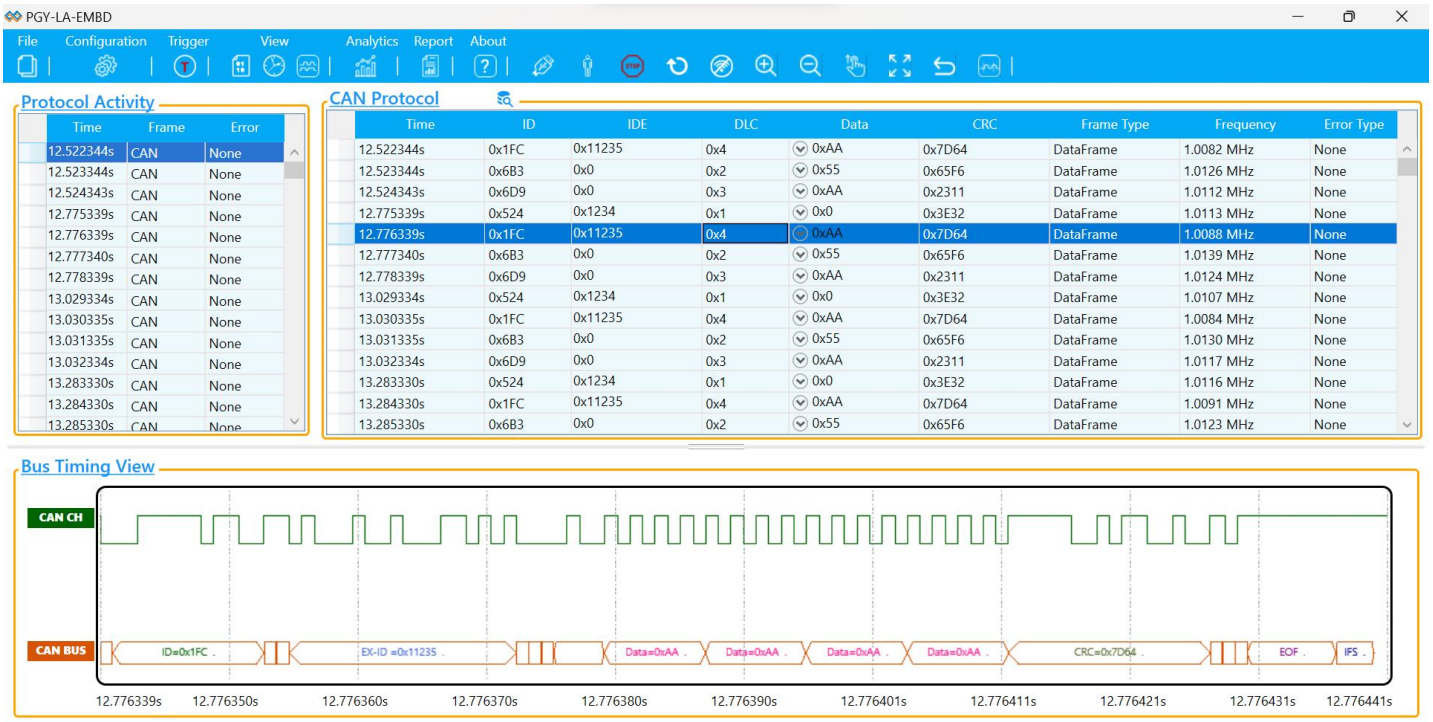
State View/Waveform Listing View



State view helps designers to see the actual signal behavior. Using the device clock as reference, it provides the plot of clock and data signals with bus diagram. Grouping of signals ensures designers have the flexibility to view signals together. All signals are time correlated to help look into setup and hold times, pulse width, missing data, etc. which are very critical for digital designs as designers look to optimize their codes.

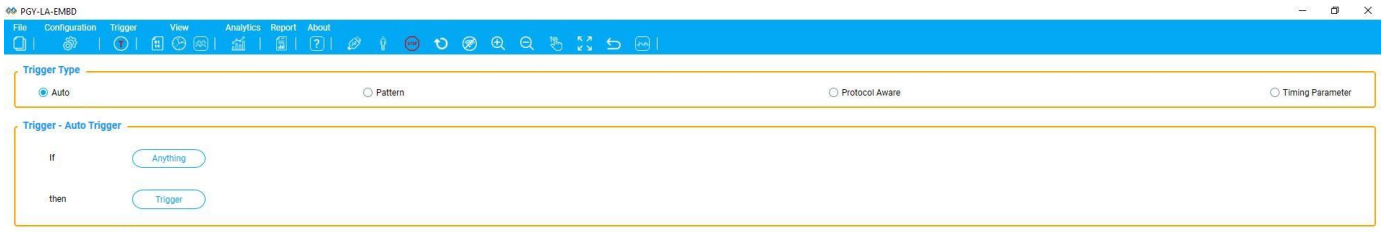
Protocol Decode View





Protocol Activity window provides the decoded packet information in each state and all packet details with error info in the packets. This gives the system level insight to the design teams. The individual protocol decodes windows based on selected interfaces ensuring easy view ability for design teams. The Selected frame in Protocol listing window will be auto correlated in timing view to view the timing information of the packet. Protocol errors will be highlighted to ensure designers are alerted to the sameeasily.

Powerful Trigger Capabilities



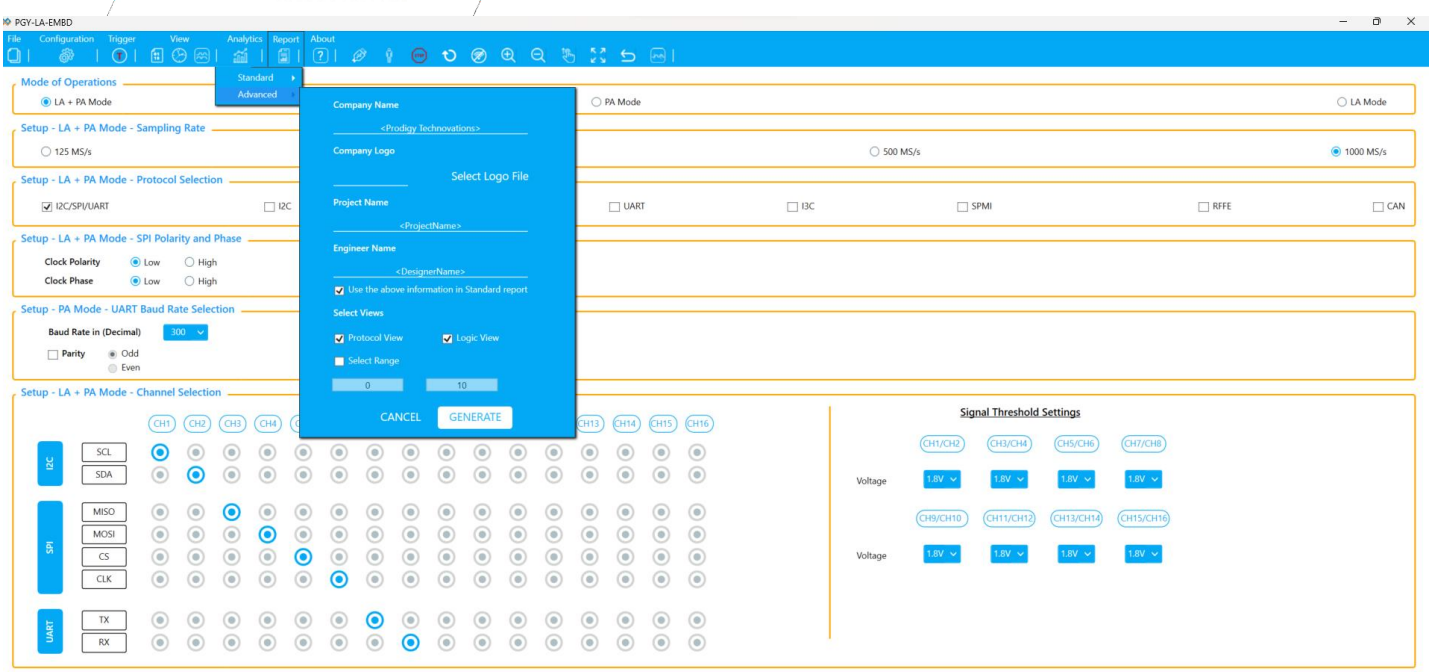
PGY-LA-EMBD supports Auto, Pattern, Protocol Aware and Timing Parameter trigger capabilities. Users can trigger on any of the Protocol packets. Comprehensive Trigger provides the flexibility to monitor different conditions.

Analytics

Detailed analytics on various protocols to enable better analysis and provide additional insights to designers

Report

Report can be generated in PDF or CSV format with details of all the signal information, plots and custom details like name of the company, logo, tester name, date and time to ensure designers can document all details and share the report.



PGY-LA-EMBD Specification

Specification	Features
No of Channels	16 Logic Channels
State Speed	100MHz (Synchronous Capture)
Timing Speed	1GS/s (Asynchronous Capture)
Number of state clock support	Two, Flexibility to sample on rising or falling edge
Record Length	Smart Continuous streaming of data to HDD/SSD of host computer
Voltage Level Support	0 to 5V with Flexibility to define the logic threshold
Waveform Plot	Plots waveforms with flexible configurable bus diagram
Listing View	List all the data samples at each sampling point
Trigger for LA	Pattern Trigger, Pulse width trigger, Delay trigger
Protocol Decode Support	I2C, SPI, UART, I3C, SPMI, RFFE, CAN, and CAN FD
Simultaneous Protocol Decoding	**Yes**, Users can analyze multiple protocols simultaneously. E.g., Users can analyze I2C, SPI, and UART bus simultaneously and capture the bus data and displays it in a time-correlated view with the corresponding time waveforms.
Protocol View with timingview (PA+LA)	Displays the protocol-decoded data with a high samplerate and timing waveform at the same time

API Support	Support for Automation of Operation using Python
Connector type	Flying Lead Probe with Female Connectors #16 Micro Grabber Test Clips as Optional Accessories
External Triggers	Trigger Out SMA Connector
Markers	Six, with delta information between two markers.
Views	Timing View State/Logic/Waveform Listing ViewProtocol View Bus-Diagram to display Protocol packets with timing. diagram plot Auto Trigger – Default (Trigger on anypacket)
Protocol Trigger	Pattern Trigger ProtocolAwareTrigger- **UART**: Start bit, Parity Bit, Data **SPI**: MOSI Data, MISO data **I2C**: START bit, Address, Data, Address plus Data, ACK,NACK, Repeated START, STOP bit. **I3C**: Broadcast command, Ack, NACK, Directed, Slave address, read, write. **SPMI:** Command, Slave/MID, Byte count, Register address, Data. **RFFE**: Command, Slave/MID, Byte count, Register address, Data. **CAN**: ID, EXT- ID, DLC, Data **Timing parameter trigger**: Pulse width (Positive orNegative) Delay Trigger
Capture duration	Smart streaming of Protocol Data to host HDD/SSD
Report	Report Generation in PDF and CSV format
Host Connectivity	USB 3.0 Type-C
Dimensions	115mmx90mmx25mm
Weight	300g

Ordering Information

PGY-LA-EMBD (v 1.0): Logic Analyzer for Embedded Interfaces.

Deliverables for PGY-LA-EMBD

PGY-LA-EMBD Unit.
USB 3.0 cable.
5V DC Power Supply.
PGY-LA-EMBD Software in CD.
Flying lead probe cable with female connector to connect to DUT.

Optional Accessories

PGY-LA-EMBD-Cable: Flying lead probe cable with female connector to connect to DUT Micro Grabber Test Clips (#16 Nos).

Contact Information

About Prodigy Technovations Pvt Ltd

Prodigy Technovations Pvt Ltd (www.prodigytechno.com) is a leading global technology provider of Protocol Decode, and Physical layer testing solutions on test and measurement equipment. The company's ongoing efforts include successful implementation of innovative and comprehensive protocol decode and physical layer testing solutions that span the serial data, telecommunications, automotive, and defense electronics sectors worldwide.