

PGY-PCIeGen3/4-PA

PCIe Protocol Analyzer (upto Gen 4 Datarates)



The PGY-PCIeGen3/4-PA is a PCIe Protocol Analyzer that supports protocol analysis up to PCIe Gen4 speeds. PCIe design and test engineers can easily captures and record traces at 2.5, 5.0, 8 and 16GT/s at specific event and obtain error report instantaneously at affordable price. This enables the design and test engineers to reduce the development time and address the time to market needs. PCIe Gen4 data is captured using interposers between the root complex and end point (Device under test). PCIe Gen4 interposers support. PCIe Gen4 Protocol Analyzer's software provides complete decode and error analysis of Transaction Layer Packets (TLPs), data link Layer Packets and with LTSSM information.

PGY-PCIeGen3/4-PA software provides powerful protocol decode capabilities enabling engineers to quickly identify the problems in protocol layer. Software is capable of decoding the packets and provide error analysis. Different views of Protocol layer enables the user to quickly identify the problems in protocol. Power search, filter-in, filter-out features simplify debug activity.

PGY-PCIeGen3/4-PA provides sophisticated protocol trigger features which allows trigger on specific protocol event and capturing the data of interest. Auto, simple and advanced trigger features capture PCIe bus activity, specific event and monitor multiple trigger conditions and capture data around it.



Key features

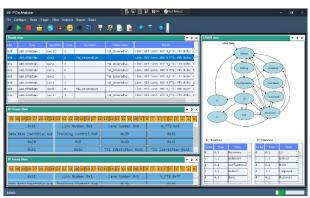
- PCIe Gen1/2/3/4-X4 Protocol Decode and Analysis.
- Currently supports four lane PCleGen1/2/3/4 Bus.
- Active M.2 Connector interposer for speeds up to PCIe Gen4 is standard offering with protocol analyzer.
- Optional Passive M.2 Connector interposer for speeds up to PCIe Gen3.
- Optional solder down probe tips for four lanes for speeds up to PCle Gen3 (8Gbps)
- Protocol Decoding of TS1, TS2, TLP, DLLP Packets.
- Hardware based protocol packet TS1, TS2 and IDLE filter capabilities.
- Software based search, filter-in and filter-out capabilities.
- Hardware based protocol aware trigger capabilities.
- Advanced multi-level if-then-else if trigger capabilities.
- Standard buffer size of 16GB and expandable to 64GB combined for TX and RX.
- Trigger based on TS1, TS2, TLP and DLLP Packet content.
- Detailed view of each TLP/DLLP with all field values.
- LTSSM Analysis for PCIe protocol traffic.
- Memory segmentation with each segment with different trigger condition¹.
- Trigger out signal at trigger event allows the triggering of other instruments such as an oscilloscope.
- Interface to host system using USB 3.0.
- Decoded data packets can be exported to .txt file for further analysis.
- PGY Protocol Analyzer is light weight and can be deployed for on-site/ field tests.
- Field upgradeable enables the unit to easy maintain for latest feature set.

			Lane	Upstream		
19076307	2.8925s	Gen3	2		SKP_OrderedSet	
19076308	2.8925s	Gen3	3		SKP_OrderedSet	
19076309	2.8925s	Gen3			IDL	64
19076310		Gen3				CfgNr0 - Configuration Write Type 0 Seq# 1
19076311	2.8925s	Gen3		IDL		56
19076312	2.8925s	Gen3			DLLP	Type: Ack
19076313	2.8925s	Gen3			IDL	48
19076314	2.8925s	Gen3			TLP	Cpl - Completion without Data Seg# 1
19076315	2.8925s	Gen3			DLLP	Type: UpdateFC-NP
19076316	2.8925s	Gen3			IDL	48
19076317	2.8925s	Gen3			DLLP	Type: Ack
19076318	2.8925s	Gen3			IDL	48
19076319	2.8925s	Gen3		DLLP		Type: Ack
19076320	2.8925s	Gen3		IDL		56
19076321	2.8925s	Gen3		DLLP		Type: UpdateFC-Cpl
19076322	2.8925s	Gen3		IDL		56
19076323	2.8925s	Gen3		TLP		CfgRd0 - Configuration Read Type 0 Seq# 2
19076324	2.8925s	Gen3		IDL		76
19076325	2.8925s	Gen3			TLP	CplD - Completion with Data Seq# 2
19076326	2.8925s	Gen3			DLLP	Type: UpdateFC-NP
19076327	2.8925s	Gen3			IDL	48

	🚈 😵 🏮	Analytics Report	7beut	B 🖪 💉	7 0						
lesult všew	India I			/-	-		Q X LISS	M view			- 0
								88.X 2	10		
58,0722211246	Ger3		TOL.	8			-		Cond		
58.0722211275 Gen3			0000	Type: Ack Seq #2581				1	Fred	1	1
58.0722211276	8.0722211275 6013 200		TOL	a .						1	1
53,0722211315	Co13		TLP		d Request Sept 261	ion necessas(necesis) to	3	1		W.	
58.0722211396	So Gena IDL		IDL	26				1	V	1	1
58.0722211375		TEP		Chin - Condistino with Data Selfs SSB CCC 892535399V(092535089V) In-					Contiguation	1 (10	- 2/\
51.0722211425	Ger3		TLP	FRG - Newcry Rea	ii Request Sept 262	LCRC 0x0788FF12(8x8708FF32) Tru	2.	1	I	1	211
	1000		(0)77/2	10				-	-	la la	aut)
Frame View							×	1	THE	117	11
									the same	1	V
								-6	-		
1 30 29 2	8 27 26 25 2	23 22 21 2	0 19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4 3 2 1	0	1	0	1	7
1 30 29 2: Frame View	8 27 26 25 2	23 22 21 2	0 19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4 3 2 1	9 (3	0	>	7
1 30 29 2 Frame View	8 27 26 25 2	23 22 21 2	0 19 18 17 16	15 14 13 12	11 10 9 8		v ×	Ð,	0	>	7
1 30 29 2	8 27 26 25 2 8 27 26 25 2	23 22 23 2	0 19 18 17 18 0 19 18 17 18	15 14 13 12	11 10 9 8	7 6 5 4 3 2 1	ų ×			>	,
1 30 29 2 Luga (20) 80			0 19 18 17 10 0 19 18 17 10 5th[10:4] 0x0	15 14 13 12 15 14 13 12 FORE 6X2		7 6 5 4 3 2 1 ense No. 8x185	ų ×	January Company		Lir State	Mos
Frame View 12 30 29 2 12 30 29 2 13 30 30 30 30 14 40 80	8 27 26 28 24 8 27 26 25 24 8 27 26 25 24 8 27 8 28		0 19 18 17 16 0 19 18 17 16 5th[16:4] 0x8 6x3	15 14 13 12 15 14 13 12 FCRC 6x2		7 6 5 4 3 2 1	0 X	Time		>	Mos
1 30 29 2 Lingu (20) 80 R 405 8X1					(0	7 6 5 4 3 2 1 ense No. 8x185	0 X	Time	Social dest	LF State	Now State
2 30 29 2 Luga (20 00 6 400 8x1	NRs 8x8		0x8	8	3	7 6 5 4 7 2 1 ence No. 8x105 0x88	0 X	1.1 E	dert .	LF State	Mos Stra
1 30 29 2 togu(20) 00 t 404 9x1	NR# 8x8 8x3		0x8 0x8	6: 8:	(3 (8	7 6 5 4 3 2 1 ence No. 8x105 0x86 0xFF	0 K.	10.1 E	dert .	B 3000	Mos Stratte Brante









	Specifications				
Data Rates Supported	PCIe Gen1, Gen2, Gen 3, Gen 4. (with Option PCIe4)				
Link Width	Four lanes (Four TX and Four RX).				
Probes	Active M.2 Interposer (Standard) Solder Down Active Probes for speeds up to PCIe Gen3. (Optional)				
Protocol Decode	TS1, TS2, TLP, DLLP,SDS, IDLE, EIOS, EIEOS, FTS, SKP				
Trace Capture Size	Supports Continuous streaming of Protocol data to Host computer SSD/HDD. And Post Capture up to buffer size.				
Trigger	Based on TS1, TS2, TLP, DLLP.				
Connectors	Interface for Active probes. Trigger in/out SMA connectors.				
Interface for Host Computer	USB 3.0.				
Host Computer Requirements	Processor: Intel i7 10 th Generation or better (Equivalent) Operating System: Windows 7/8.0/8.1/10 64bit OS. RAM: minimum 16GB but the product would give a faster response for 32GB/64GB/more. Storage: 256GB SSD or more (minimum storage capacity of 1GB should be available in the hard disk drive. User can use more storage based on trace storage requirement.) Display resolution: 1024X768. Interface: Host computer should support USB 3.0 interface.				
Dimension (W x H x D)	(W x H x D) (20.5X5X25) cms.				
Weight	Approx. 4 kg.				
Power Requirement	12V, 6A DC Power Supply (AC/DC Supplied along with Analyzer).				

Ordering information:

PGY-PCleGen3/4-PA: PCle Gen3/4 Protocol Analyzer

Note: Unit by default supports up to Gen 3 data rates. For Gen4 support, please include Opt PCle4 at time of ordering. (Shipment includes Hardware, software CD, One Active M.2 Interposer, USB 3.0 Cable and Power adapter)

Opt PCle4: Add PCleGen4 support

Post Purchase Upgrade:

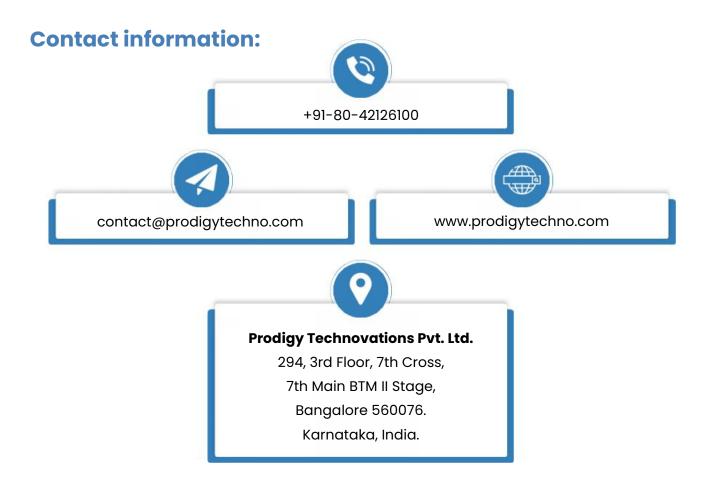
PGY-UPG-Gen3/4 Upgrade to PCleGen 4 from PCleGen3

(Shipment includes Hardware, software CD, One Active M.2 Interposer, USB 3.0 Cable and Power adapter)



Warranty:

12 Months of Hardware Warranty & Software upgrade Support (Accessories, Interposer, Probes are covered for a 90 Days warranty only against any manufacturing defects)



About Prodigy Technovations Pvt Ltd

Prodigy Technovations is the leading provider of innovative protocol analysis solutions for mainstream and emerging technologies. We provide Protocol Decode, and PHY layer testing solutions on Test & Measurements equipment's. The company's ongoing efforts include successful implementation of innovative and comprehensive protocol Analysis solutions using latest hardware technologies.